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**TITLE**

**COLLAR DIELECTRIC PROCESS FOR REDUCING A TOP WIDTH OF A DEEP**  
**TRENCH**

**BACKGROUND OF THE INVENTION**

**5 Field of the Invention**

The invention relates to a deep trench capacitor, and more particularly to a collar dielectric process for a deep trench capacitor in order to reduce the top width of the deep trench.

**10 Description of the Related Art:**

A DRAM cell comprises a transistor coupled to a capacitor. Currently in the semiconductor industry, DRAM cell includes a deep trench capacitor and a planar transistor. The deep trench capacitor is a three dimensional structure formed in a silicon substrate, and has the advantages of smaller memory area, lower power consumption and higher operating speed.

FIG. 1A is a plane view illustrating the arrangement of deep trenches, word lines and bit lines in a conventional DRAM cell. For a folded bit line structure, each active area comprises two word lines WL<sub>1</sub> and WL<sub>2</sub> and one bit line BL, in which the character "DT" indicates the deep trench, and the character "BC" indicates a bit line contact.

FIG. 1B is a cross-section illustrating a conventional deep trench capacitor of a DRAM cell. A deep trench DT is formed in a silicon substrate 10, and a deep trench capacitor 12 is formed in the lower portion of the deep

trench DT. The deep trench capacitor 12 is composed of a buried plate, a node dielectric and a storage node. The conventional method of forming the deep trench capacitor 12 employs the following steps. First, a reactive ion etching 5 (RIE) method is used to form the deep trench DT in the p-type silicon substrate 10. A high-temperature and short-term annealing process using a heavily-doped oxide material (such as ASG) is performed.  $N^+$  ions are diffused into the silicon substrate 10 at the lower portion of the deep trench 10 DT, thus forming an  $n^+$ -type diffusion region 14 to serve as the buried plate of the deep trench capacitor 12. Next, a silicon nitride layer 16 is formed on the sidewall and bottom of the lower portion of the deep trench DT to serve as the node dielectric of the deep trench capacitor 12. 15 Next, a first  $n^+$ -doped polysilicon layer 18 is deposited to fill the deep trench DT after which it is recessed to reach a predetermined depth, thus serving as the storage node of the deep trench capacitor 12.

After completing the deep trench capacitor 12, a collar 20 dielectric layer 20 is formed on the sidewall of the upper portion of the deep trench DT, after which a second  $n^+$ -doped polysilicon layer 22 is deposited to fill the deep trench DT. Then, a third polysilicon layer 24 is formed over the second polysilicon layer 22. Subsequently, processes for 25 STI (shallow trench isolation) structure 26, the word lines WL<sub>1</sub> and WL<sub>2</sub>, a source/drain diffusion region 28, and the bit line contact BC and the bit line BL are performed thereon. The STI structure 26 is used to isolate two adjacent DRAM cells.

In addition, a buried strap outdiffusion region 30 is formed in the silicon substrate 10 at the top portion of the deep trench DT for connecting the deep trench capacitor 12 to a planar transistor. Thus, the buried strap outdiffusion region 30 is also called a node junction. Typically, using thermal annealing, the  $n^+$  ions of the second polysilicon layer 22 can diffuse into the silicon substrate 10 through the third polysilicon layer 24 to form the buried strap outdiffusion region 30. Thus, the third polysilicon layer 24 is also called a buried strap 24.

The collar dielectric layer 20 is required to isolate the buried strap outdiffusion region 30 from the buried plate 14 because current leakage of the buried strap outdiffusion region 30 to the buried plate 14 may degrade the retention time of the DRAM cell. The conventional method for the collar dielectric layer 20 increases the top width of the deep trench DT, which limits the WL-DT (word line to deep trench) overlay tolerance and the distribution of the buried strap outdiffusion region 30. Particularly, the increased top width of the deep trench DT reduces an overlay margin area L between the source/drain diffusion region 28 and the buried strap outdiffusion region 30, resulting in serious junction leakage and worse sub-V<sub>t</sub> performance.

FIGS. 2A to 2E are cross-sections illustrating a conventional method for the collar dielectric layer 20 shown in FIG. 1B. In FIG. 2A, the p-type semiconductor silicon substrate 10 is provided with the deep trench capacitor 12 at the lower portion of the deep trench DT. The capacitor process includes steps of forming a silicon nitride pad

layer 32, the deep trench DT, the n<sup>+</sup>-type diffusion region 14, the silicon nitride layer 16 and the n<sup>+</sup>-doped first polysilicon layer 18. Then, in FIG. 2B, the silicon nitride layer 16 is removed from the upper portion of the deep 5 trench DT, after which the first polysilicon layer 18 is recessed. Next, an oxidation process is performed to grow a first silicon oxide layer 34 on the exposed surface of the silicon substrate 10. The first silicon oxide layer 34 covers the sidewall of the upper portion of the deep trench 10 DT to ensure the isolation result between the n<sup>+</sup>-type diffusion region 14 and the buried strap outdiffusion region 30 which will be formed in subsequent processes. Next, in FIG. 2C, a chemical vapor deposition (CVD) method is employed to conformally deposit a second silicon oxide layer 15 36, after which an anisotropic dry etching method is employed to remove the second silicon oxide layer 36 from the top of the first polysilicon layer 18.

Next, in FIG. 2D, the second n<sup>+</sup>-doped polysilicon layer 22 is deposited to fill the deep trench DT, after which it 20 is recessed to reach a predetermined depth. Finally, in FIG. 2E, a wet etching method is employed to remove portions of the second silicon oxide layer 36 and the first silicon oxide layer 34 until the top of the second polysilicon layer 22 protrudes from the second silicon oxide layer 36 and the 25 first silicon oxide layer 34. Thus, the remaining portion of the second silicon oxide layer 36 and the first silicon oxide layer 34 serves as the collar dielectric layer 20.

During the oxidation process for growing the first silicon oxide layer 34, a part of the silicon substrate 10 30 is converted into SiO<sub>2</sub>, thus the top width of the deep

trench DT is increased through the subsequent wet etching process. This reduces an overlay margin area L between the source/drain diffusion regions 28 and the buried strap outdiffusion region 30, resulting in serious junction 5 leakage and worse sub-Vt. The oxidation process for the first silicon oxide layer 34 is the main factor in increasing the top width of the deep trench DT, but is important nonetheless, and cannot be skipped as more serious junction leakage will occur if the first silicon oxide layer 10 34 is thinned or omitted. Accordingly, based on the prerequisite oxidation for the first silicon oxide layer 34, a novel collar dielectric process of reducing the top width of the deep trench DT is called for.

#### **SUMMARY OF THE INVENTION**

15 Accordingly, an object of the present invention is to provide a collar dielectric process with an ion implantation process for selectively growing a silicon oxide layer on the sidewall of a deep trench outside a buried strap outdiffusion region.

20 According to the object of the invention, a collar dielectric process for reducing a top width of a deep trench has the following steps. A semiconductor silicon substrate has a deep trench and a deep trench capacitor. The deep trench capacitor has a node dielectric formed on the 25 sidewall and bottom of the deep trench, and a storage node formed in the deep trench and reaching a predetermined depth. An ion implantation process is performed to form an

ion implantation area on the substrate at the top of the deep trench. The node dielectric is then removed until the top of the node dielectric is leveled off with the top of the storage node, thus exposing the sidewall of the deep 5 trench outside the deep trench capacitor. Next, an oxidation process is performed to grow a first silicon oxide layer on the exposed sidewall of the deep trench, in which the first silicon layer is outside the ion implantation area.

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#### DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

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FIG. 1A is a plane view illustrating the arrangement of deep trenches, word lines and bit lines in a conventional DRAM cell.

FIG. 1B is a cross-section illustrating a conventional deep trench capacitor of a DRAM cell.

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FIGS. 2A to 2E are cross-sections illustrating a conventional method of forming the collar dielectric layer 20 shown in FIG. 1B.

FIGS. 3A to 3F are cross-sections illustrating a collar dielectric process of the present invention.

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FIG. 4A is a cross-section illustrating a DRAM cell with the collar dielectric layer shown in FIG. 3F.

FIGS. 4B and 4C are plane views illustrating the arrangement of deep trenches, word lines and bit lines of the DRAM cell shown in FIG. 4A.

#### DETAILED DESCRIPTION OF THE INVENTION

5 The present invention is a collar dielectric process for reducing a top width of a deep trench over a deep trench capacitor. Also, the collar dielectric process ensures the isolation result between a buried strap outdiffusion region at the top of the deep trench and a buried plate at the  
10 lower portion of the deep trench so as to prevent damages to the sub-V<sub>t</sub> performance from leakage therebetween. Preferably, the collar dielectric process is applied to a DRAM cell including a transistor coupled to a deep trench capacitor, in which the transistor is a planar or vertical  
15 type.

FIGS. 3A to 3F are cross-sections illustrating a collar dielectric process of the present invention.

In FIG. 3A, a deep trench DT is formed in a silicon substrate 40, and a deep trench capacitor 42 is completed at  
20 the lower portion of the deep trench DT. The formation of the deep trench capacitor 42 composed of a buried plate, a node dielectric and a storage node employs the following steps. First, using a reactive ion etching (RIE) method with a pad layer 52 as a pattern mask, the deep trench DT is  
25 formed in the p-type silicon substrate 40. Then, using a heavily-doped oxide material (such as ASG) with a high-temperature, short-term annealing process, n<sup>+</sup> ions are diffused into the silicon substrate 40 at the lower portion of the deep trench DT, thus forming an n<sup>+</sup>-type diffusion

region 44 as the buried plate of the deep trench capacitor 42. Next, a silicon nitride layer 46 is deposited on the sidewall and bottom of the lower portion of the deep trench DT. Next, a first n<sup>+</sup>-doped polysilicon layer 48 is 5 deposited to fill the deep trench DT after which it is recessed to reach a predetermined depth, thus serving as the storage node of the deep trench capacitor 42. The silicon nitride layer 46a formed at the lower portion of the deep trench DT and sandwiched between the buried plate and the 10 storage node serves as the node dielectric of the deep trench capacitor 42.

In FIG. 3B, before removing the silicon nitride layer 46b from the upper portion of the deep trench DT, an ion implantation process 54 is performed with the silicon nitride layer 46 as a screen layer to form an ion impanation area 56 in the silicon substrate 40 at the top portion of the deep trench DT. Preferably, the position and vertical length I of the ion implantation area 56 substantially correspond to those of a buried strap outdiffusion region 20 which will be formed in subsequent processes. Preferably, the ion implantation process 54 uses a tilt-angle implantation with N<sub>2</sub> as the ion source, and the vertical length I of the ion impanation area 56 is approximately 800~1500Å.

25 In FIG. 3C, the silicon nitride layer 46b is removed from the upper portion of the deep trench DT, after which a first silicon oxide layer 51 is grown on the exposed surface of the silicon substrate 40 through an oxidation process. It is noted that the above-described ion implantation process 54 restrains the silicon substrate 40 at the top of 30

the deep trench DT from converting into  $\text{SiO}_2$  during the oxidation process, thus the first silicon oxide layer 51 is merely grown on the exposed silicon substrate 40 outside the ion implantation area 56. The first silicon oxide layer 51 5 ensures the isolation result between the  $n^+$ -type diffusion region 44 and a buried strap outdiffusion region which will be formed in subsequent processes.

In FIG. 3D, using a CVD method or other deposition processes, a second silicon oxide layer 53 is conformally 10 deposited on the sidewall and bottom of the deep trench DT. Then, a dry etching method is used to remove the second silicon oxide layer 53 from the top of the first polysilicon layer 48.

In FIG. 3E, a second  $n^+$ -doped polysilicon layer 58 is 15 deposited to fill the deep trench DT, after which it is recessed to reach a predetermined depth.

In FIG. 3F, using a wet etching method, portions of the second silicon oxide layer 53 and the first silicon oxide layer 51 are removed and leveled with each other until the 20 top of the second polysilicon layer 58 protrudes from the second silicon oxide layer 53 and the first silicon oxide layer 51. Thus, the combination of the second silicon oxide layer 53 and the first silicon oxide layer 51 remaining on the sidewall of the deep trench DT serve as a collar 25 dielectric layer 50.

FIG. 4A is a cross-section illustrating a DRAM cell with the collar dielectric layer 50 shown in FIG. 3F. After completing the collar dielectric layer 50, the following steps of forming a third polysilicon layer 60 (also called a 30 buried strap), a buried strap outdiffusion region 62, an STI

structure 64, two word lines  $WL_1$  and  $WL_2$ , a source/drain diffusion region 66, a bit line contact BC and a bit line BL are performed thereon.

According to the above-described collar dielectric process, the ion implantation area 56 is formed corresponding to the buried strap outdiffusion region 62 before removing the silicon nitride layer 46b, and the first silicon oxide layer 51 is selectively grown on the silicon substrate 40 outside the buried strap outdiffusion region 62, thus the wet etching process for removing the first silicon oxide layer 51 does not increase the top width of the deep trench DT.

Compared with the conventional collar dielectric method which increases the top width of the deep trench, it has been experimentally proven that the collar dielectric process of the present invention can reduce the top width of the opening radius of the deep trench to 40~60Å. Thus, an overlay margin area L between the source/drain diffusion region 66 and the buried strap outdiffusion region 62 is reduced so as to solve the junction leakage problem and improve the sub-V<sub>t</sub> performance. Additionally, the only modification to the conventional collar dielectric process required by present invention is the ion implantation process 54 for the ion implantation area 56. The process is further simplified by not requiring an extra photoresist patterning process for the above mentioned ion implantation process and performs other steps as usual. Thus the invention has the advantages of a simplified procedure, low process cost, and is well suited to mass production.

FIGS. 4B and 4C are plane views illustrating the arrangement of deep trenches DT, word lines WL<sub>1</sub> and WL<sub>2</sub>, a bit line contact BC and a bit line BL of the DRAM cell shown in FIG. 4A. In one embodiment of the present invention, as shown in FIG. 4B, the ion implantation area 56 partially surrounds the top of the deep trench DT and is adjacent to the second word line WL<sub>2</sub>. In the other embodiment of the present invention, as shown in FIG. 4C, the ion implantation area 56 entirely surrounds the top of the deep trench DT.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.